

<p>CTKD7N65SE</p> <p>Features:</p> <ul style="list-style-type: none"> <input type="checkbox"/> Low Intrinsic Capacitances. <input type="checkbox"/> Excellent Switching Characteristics. <input type="checkbox"/> Extended Safe Operating Area. <input type="checkbox"/> Unrivalled Gate Charge :Qg=29nC (Typ.). <input type="checkbox"/> $V_{DSS}=650\text{ V}, I_D=7\text{ A}$ <input type="checkbox"/> $R_{DS(on)} : 1.35\Omega$ (Max) @$V_G=10\text{ V}$ <input type="checkbox"/> 100% Avalanche Tested 	<p>TO-252</p> <div style="text-align: center;"> </div> <div style="text-align: center;"> </div> <div style="margin-top: 10px;"> <p>1.Gate (G) 2.Drain (D) 3.Source (S)</p> </div>
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Absolute Maximum Ratings (Ta=25°C unless otherwise noted)

Sy mbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	650	V
I_D	Drain Current	$T_j=25^\circ\text{C}$	7.0
		$T_j=100^\circ\text{C}$	4.7
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note1)	300	mJ
I_{AR}	Avalanche Current (note2)	7.0	A
P_D	Power Dissipation ($T_j=25^\circ\text{C}$)	50	W
T_j	Junction Temperature(Max)	150	°C
T_{stg}	Storage Temperature	-55~+150	°C
TL	Maximum lead temperature for soldering purpose,1/8' from case for 5 seconds	300	°C

Thermal Characteristics

Sy mbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance,Junction to Case	-	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance,Junction to Ambient	-	62.5	°C/W

Electrical Characteristics (Ta=25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu A, V_{GS}=0$	650	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D=250\mu A$, Reference to 25°C	-	0.67	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=650V, V_{GS}=0V$	-	-	10	μA
		$V_{DS}=520V, T_J=125^\circ C$	-	-	100	
I_{GSSF}	Gate-body leakage Current, Forward	$V_{GS}=+30V, V_{DS}=0V$	-	-	100	nA
I_{GSSR}	Gate-body leakage Current, Reverse	$V_{GS}=-30V, V_{DS}=0V$	-	-	-100	
On Characteristics						
$V_{GS(TH)}$	Gate Threshold Voltage	$I_D=250\mu A, V_{DS}=V_{GS}$	2	-	4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$I_D=3.5A, V_{GS}=10V$	-	1.25	1.35	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0, f=1.0MHz$	-	1000	-	μF
C_{oss}	Output Capacitance		-	95	-	
C_{rss}	Reverse Transfer Capacitance		-	2.4	-	
Switching Characteristics						
$T_d(on)$	Turn-On Delay Time	$V_{DD}=325V, I_D=7A, R_G=25\Omega$ (Note 3,4)	-	30	70	nS
T_r	Turn-On Rise Time		-	80	170	
$T_d(off)$	Turn-Off Delay Time		-	65	140	
T_f	Turn-Off Rise Time		-	60	130	
Q_g	Total Gate Charge	$V_{DS}=520V, V_{GS}=10V, I_D=7A$ (Note 3,4)	-	29	38	nC
Q_{gs}	Gate-Source Charge		-	7	-	
Q_{gd}	Gate-Drain Charge		-	14.5	-	
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Max. Diode Forward Current	-	-	-	7	A
I_{SM}	Max. Pulsed Forward Current	-	-	-	28	
V_{SD}	Diode Forward Voltage	$I_D=7A$	-	-	1.4	V
T_{rr}	Reverse Recovery Time	$I_S=7A, V_{GS}=0V, diF/dt=100A/\mu s$ (Note 3)	-	293	-	nS
Q_{rr}	Reverse Recovery Charge	(Note 3)	-	1.7	-	μC

- Notes : 1, L=0.5mH, IAS= 7A, VDD=50V, RG=25 Ω , Starting T_J =25°C
 2, Repetitive Rating : Pulse width limited by maximum junction temperature
 3, Pulse Test : Pulse Width \leq 300 μs , Duty Cycle \leq 2%
 4, Essentially Independent of Operating Temperature

Typical Characteristics

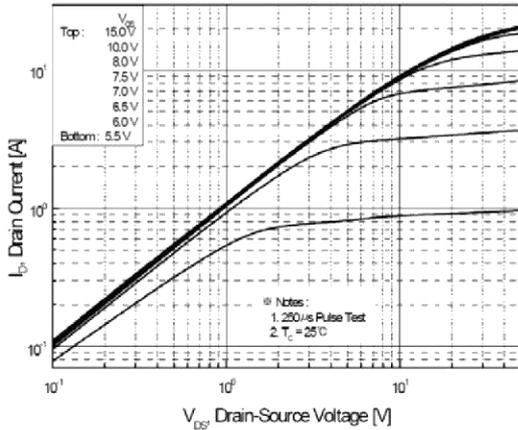


Figure 1. On-Region Characteristics

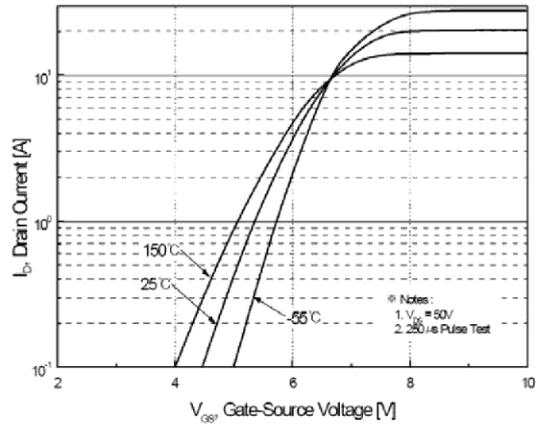


Figure 2. Transfer Characteristics

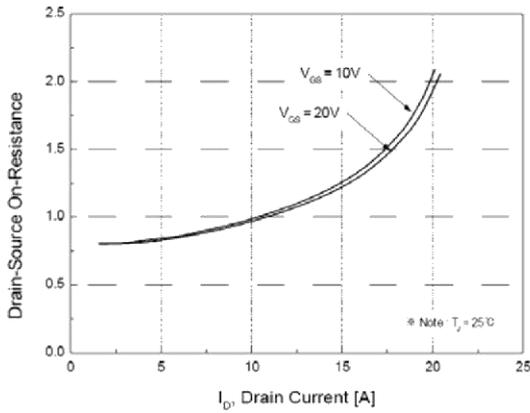


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

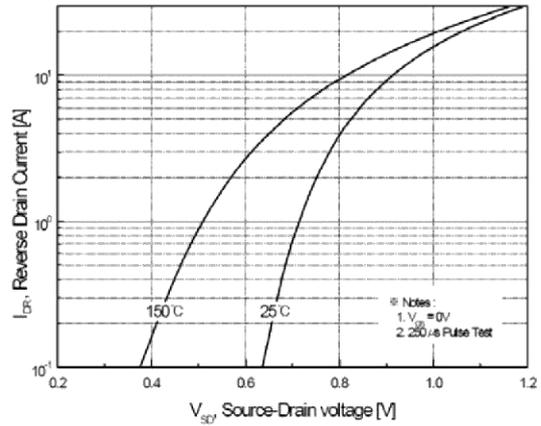


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

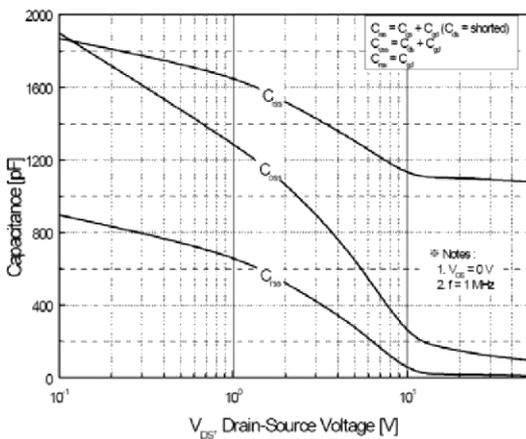


Figure 5. Capacitance Characteristics

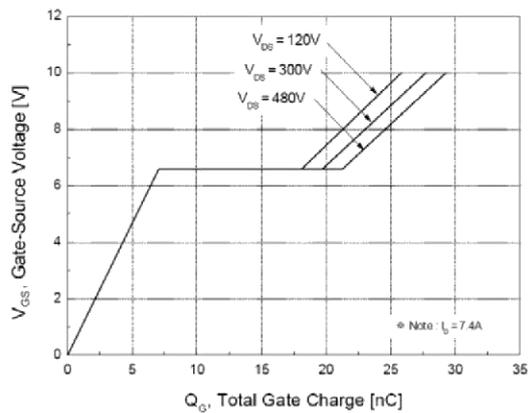


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

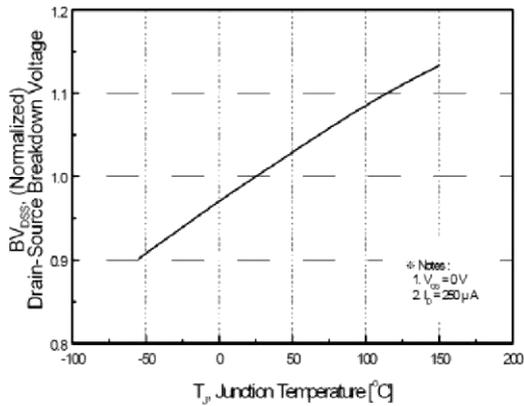


Figure 7. Breakdown Voltage Variation vs Temperature

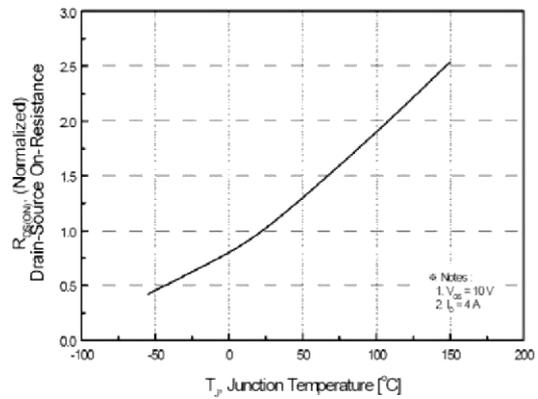


Figure 8. On-Resistance Variation vs Temperature

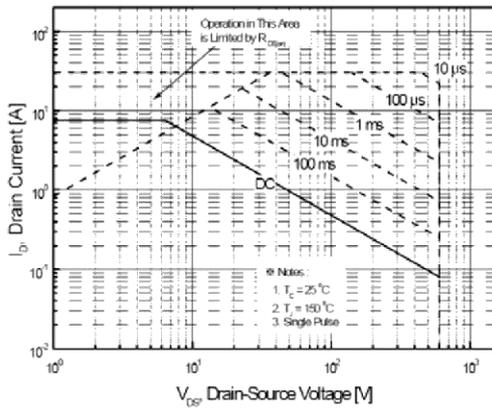


Figure 9-2. Maximum Safe Operating Area

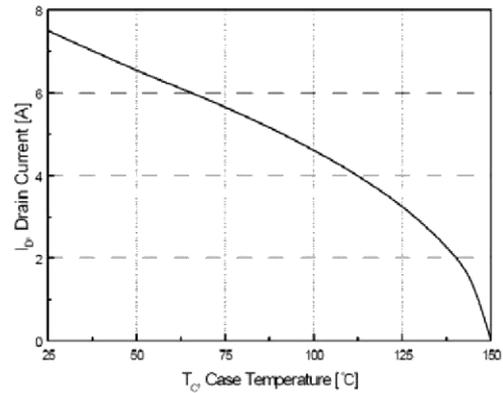


Figure 10. Maximum Drain Current vs Case Temperature

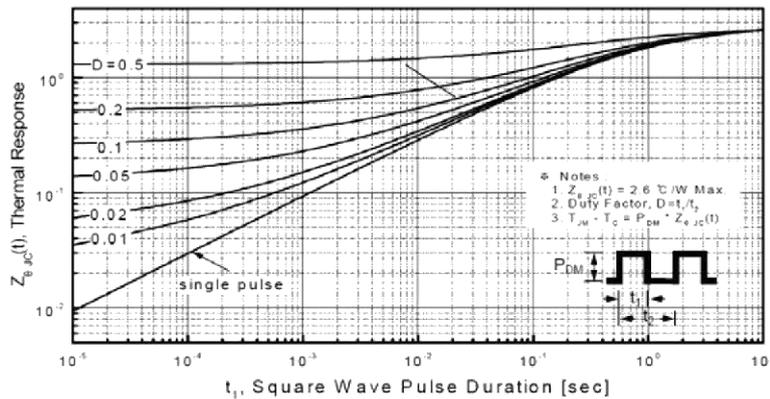
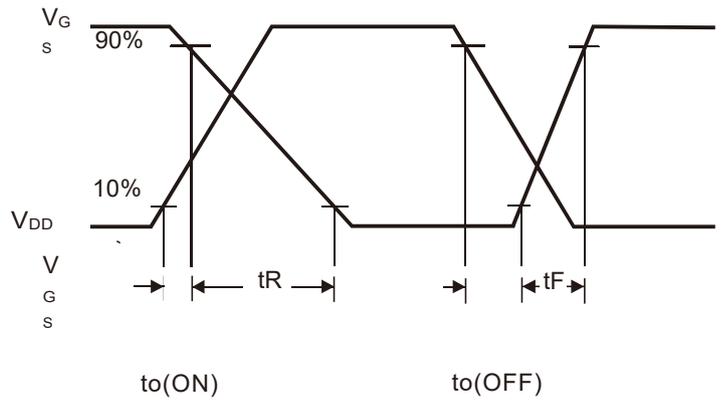
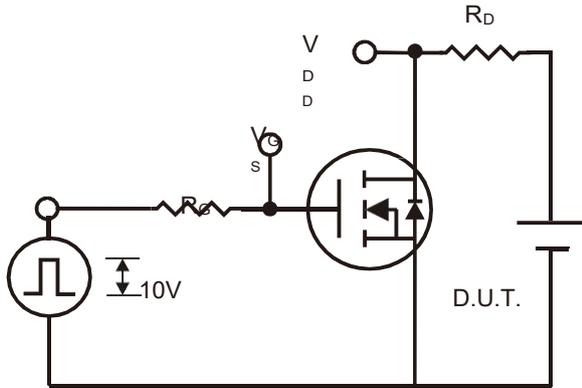
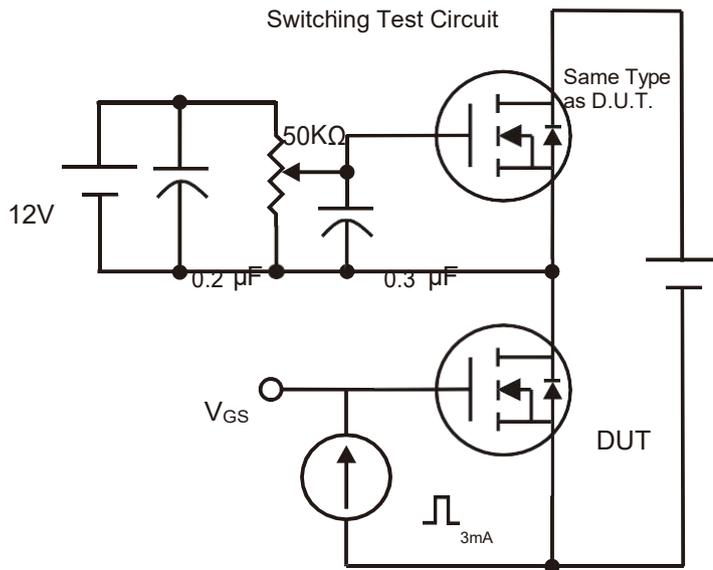


Figure 11-2. Transient Thermal Response Curve

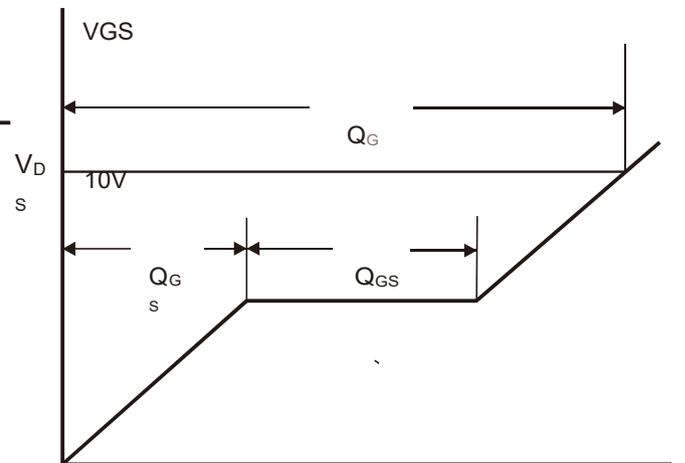
Gate Charge Test Circuit & Waveform



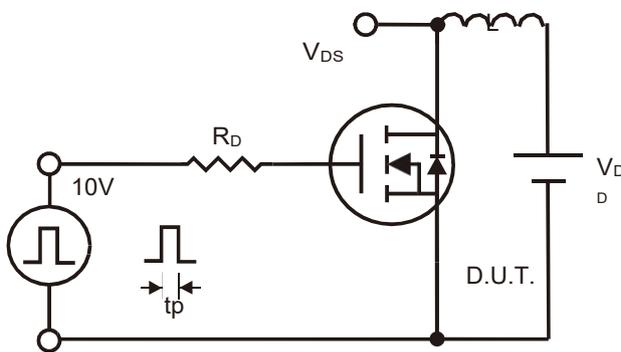
Switching Test Circuit



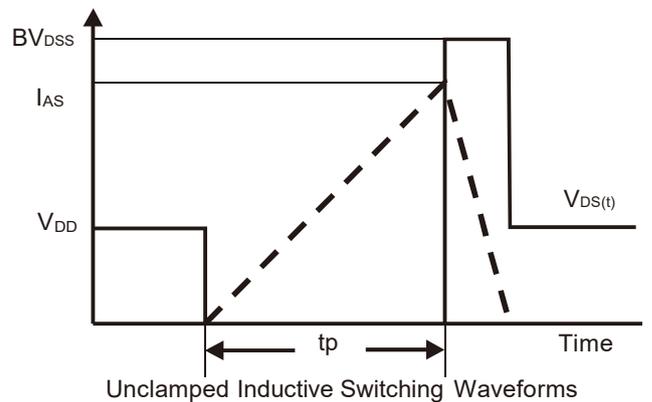
Switching Waveforms



Gate Charge Test Circuit



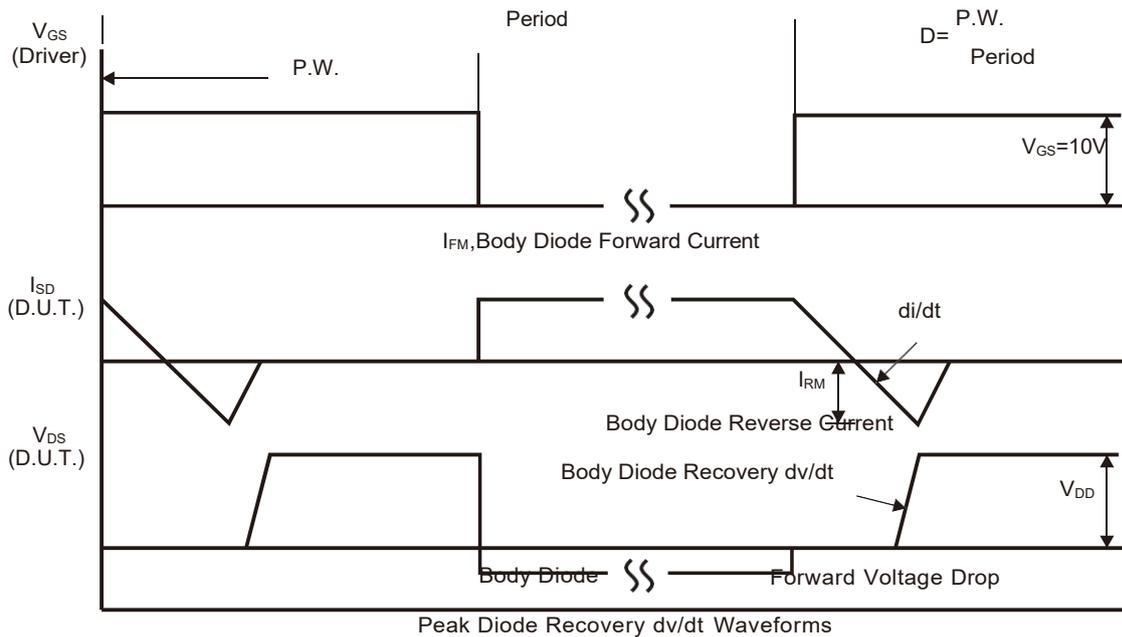
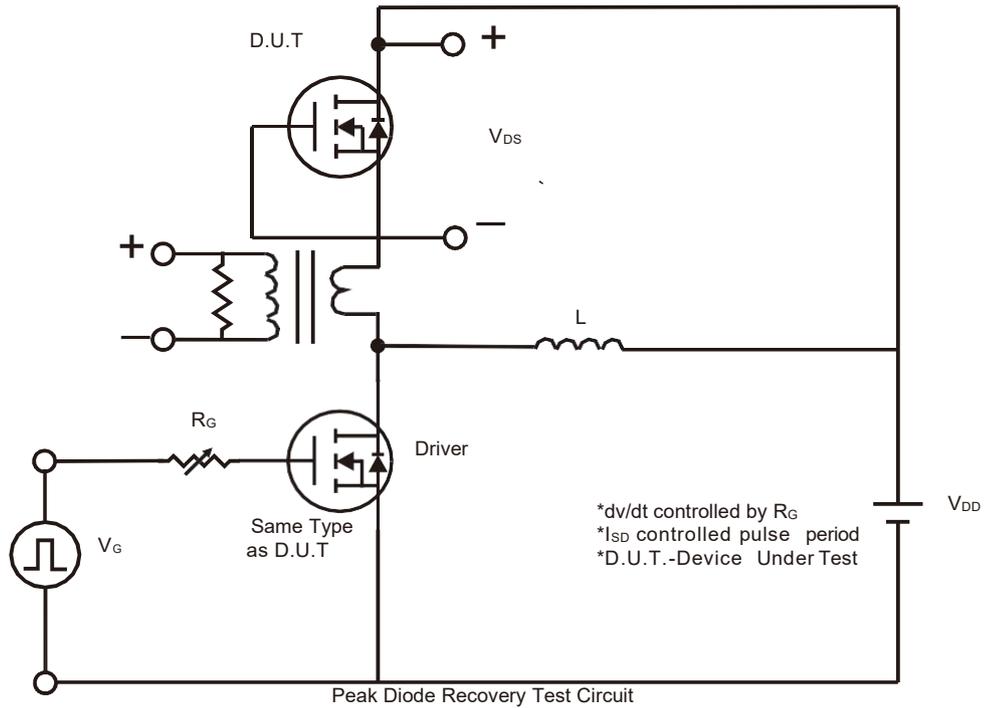
Gate Charge Waveform



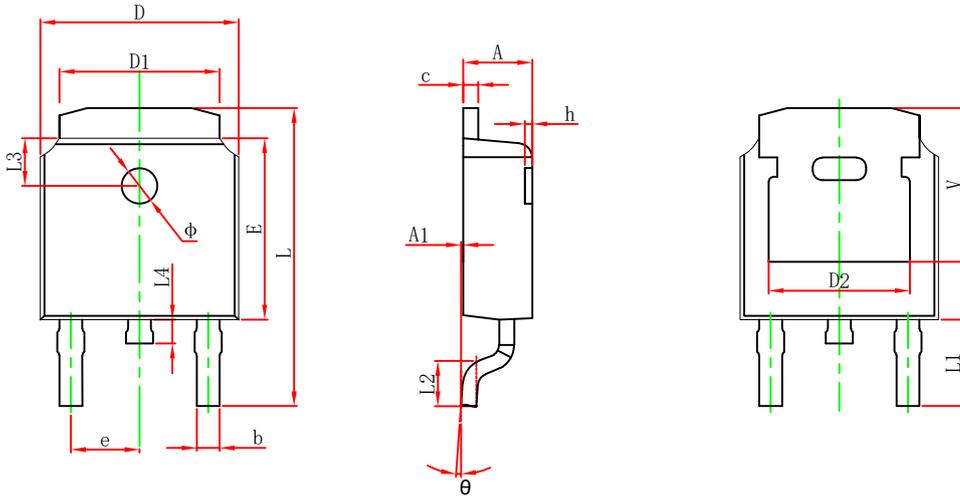
Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

Peak Diode Recovery dv/dt Test Circuit & Waveform

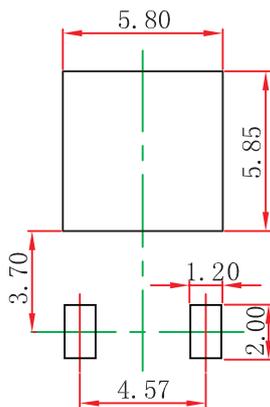


Package Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.700	0.860	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.300	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

TO-252-2L Suggest Pad Layout



NOTE:

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purposes only.